

Exhibit 11

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case No. IPR2023-00454
Patent No. 11,093,417

PATENT OWNER RESPONSE

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EX2001	Crisp, R., “Direct Rambus Technology: The New Main Memory Standard,” <i>IEEE Micro</i> , pp. 18-28 (1997)
EX2002	Datasheet for Samsung’s RIMM MR16R1624 (Wolfe Deposition Exhibit 2100)
EX2003	Deposition Transcript of Dr. Andrew Wolfe from IPR2022-00615
EX2004	Samsung Datasheet on Rambus Direct RDRAM (Dec. 2001)
EX2005	Deposition Transcript of SungJoo Park in <i>Netlist, Inc. v. Samsung Electronics Co., Ltd.</i> , 2:21-cv-00463-JRG (E.D. Tex. November 23, 2022) (excerpt)
EX2006	Ex. 7 to Park Depo
EX2007	<i>Frequently Asked Questions</i> , What is the difference between a "bank" and a "rank?", Micron, https://web.archive.org/web/20141231144416/https://www.micron.com/support/faqs (last accessed Mar. 7, 2023).
EX2008	Reserved
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EX2011	“HyperCloud HCDIMM: Scaling the High Density Memory Cliff,” July 14, 2012, downloaded from https://web.archive.org/web/20120915083048/http://www.netlist.com/media/blog/hypercloud-memory-scaling-the-high-density-memory-cliff/
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EX2013	<i>Lecture 15: DRAM Main Memory Systems</i> , University of Utah, https://my.eng.utah.edu/~cs6810/pres/11-6810-15.pdf
EX2114	“Configuring and using DDR3 memory with HP ProLiant Gen8 Servers: Best Practice Guidelines for ProLiant Servers with Intel Xeon Processors” by HP, downloaded from https://web.archive.org/web/20121023195754/http://h20000.www2.hp.com/bc/docs/support/SupportManual/c03293145/c03293145.pdf
EX2015	Ganesh, B. et al., <i>Fully-Buffered DIMM Memory Architectures: Understanding Mechanisms, Overheads and Scaling</i> , HPCA (2007)
EX2116	Datasheet for Micron DDR2 SDRAM FBDIMM MT36HTF51272FD
EX2017	U.S. Patent No. 7,356,639 (“Perego-639”)
EX2018	Redline Comparison of EX1035 (U.S. Patent No. 7,363,422 to Perego) With Related U.S. Patent No. 7,356,639
EX2019	US District Court – Judicial Caseload Profile (as of December 31, 2022)
EX2020	JESD79-2B
EX2021	Amended Docket Control Order in <i>Netlist, Inc. v. Samsung Electronics Co. Ltd.</i> , 2:22-cv-00293-JRG (E.D. Tex. Feb. 1, 2023)

EX2022	Cover pleading of Samsung's invalidity contentions in <i>Netlist, Inc. v. Samsung Electronics Co. Ltd.</i> , 2:22-cv-00293-JRG (E.D. Tex. April 13, 2023)
EX2023	IPR2023-00203, Paper 8
EX2024	Declaration of Steven Przybylski, Ph.D.
EX2025	Rambus®, Advance Information, 64/72-Mbit (256Kx16/18x16d) Direct RDRAMDirect™ Data Sheet, Modified Mar 12, 1998
EX2026	Direct Rambus™ 1.6GB/sec memory Technology Disclosure, Oct. 15, 1997
EX2027	Direct Rambus™ RIMM™ Module Specification, Version 1.0
EX2028	Samsung Electronics, 256 Mbit XDR DRAM (F-die), 2M x 16(/8/4) bit x 8s Banks, Version 1.0, Jan. 2005
EX2029	Przybylski, Steven A., "NEW DRAM TECHNOLOGIES, A Comprehensive Analysis of the New Architectures," Second Edition, ©1996
EX2030	Claim Construction Memorandum Opinion and Order, Doc. 228, Case 2:22-cv-00293, filed Nov. 21, 2023
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I. INTRODUCTION¹

Each claim of the '417 Patent requires a memory module that includes a data buffer, logic, and circuitry situated between an external memory controller and the individual memory devices on the module. The claimed logic must, among other things, receive chip-select input signals from the controller and output corresponding registered chip-select signals to the memory devices. The input chip-select signals further require chip-select lines on the module connecting the claimed logic to the external memory controller.

Neither Perego nor JESD79-2 disclose such input chip select signals or lines. Perego discloses Rambus-style modules that employ a point-to-point architecture and configurable bit-width interfaces that are fundamentally different than the conventional memory bus required by JEDEC module standards and do not include chip-select lines or otherwise convey chip-select signals. JESD79-2 is the standard for DDR2 SDRAM *memory devices*, not JEDEC *modules*, such as the JESD21-C standard for DDR2 RDIMMs. As such, its disclosure of chips-select signals relates to the connections between the on-module logic and the memory devices, not the inputs to the memory module.

Petitioner contends that because Perego discloses that one could use DDR2

¹ All emphases are added unless otherwise noted.

SDRAM memory devices in its modules, “[a] POSITA would have ... been motivated to implement Perego’s memory modules in a registered DIMM format with DDR memory devices that fits into DIMM connectors and uses DIMM module input signals, according to JEDEC standards, including JESD21-C and JESD79-2.” Pet. 32. There are several problems with this proposed combination, without which Petitioner cannot prevail on any challenged claim.

First, JESD21-C, which defines the DDR2 module, is not part of any ground identified by Petitioner. Notably, Petitioner relies on JESD21-C not just for alleged motivation to combine, but also for multiple claim elements, such as input chip-select signals that do not exist in the memory devices defined in JESD79-2. JESD21-C therefore is part of the basis on which the Petition relies, and was not properly identified as such.

Second, Perego provides a solution that avoids the need to convert its point-to-point module architecture and configurable bit-width modules into a conventional JEDEC-style bus. Specifically, Perego explains that “[d]ifferent types of memory devices may be includes on different modules within a memory system, *by employing buffer device 405 to translate protocols employed by controller 310 to the protocol utilized in a particular memory device* implementation.” EX1071, 10:63-67. In other words, Perego purportedly provides DDR2 SDRAM compatibility *without* modifying its non-JEDEC, flexible architecture, and

Petitioner identifies no compelling motivation to make such modifications. Third, modifying Perego's modules to comply with JESD21-C's RDIMM requirements would cripple core functionalities described as benefits by Perego. For example, this drastic change to Perego would defeat the very support for "new generations of memory devices while retaining backward compatibility with existing generations of memory devices" touted by Perego and relied upon by Petitioner. EX1071, 6:39-44.

At Institution, the Board observed that "Perego discloses using DDR2 memory devices." Paper 11 at 14. While JESD79-2 may inform a POSITA regarding how to interface DDR2 SDRAMs with Perego's buffer, JESD79-2 would not suggest modifying Perego's Rambus module to implement, for example, the claimed "input chip-select signals." The Institution Decision notes that "Patent Owner focuses on the lack of a chip select network, which is not recited in the claims of the '417 patent." Paper 11 at 14. The claims require a logic on the memory module "configurable to receive a set of input of address and control signals via the address and control signal lines" with the "set of input address and control signals including a plurality of input chip select signals and other input address and control signals." EX1001, 42:17-25. The input chip select signals come from off-module controllers. *Id.*, 42:7-12 (input control/address signal lines used for communicating with memory controller). The set of signal lines via which chip select signals are

transmitted is the “chip select network” discussed in EX1069 and EX1070. Perego does not implement this type of design, it has a lack of a chip select network. JESD79-2 does not disclose chip selects from the off-module memory controller to the module. In fact, it does not even mention chip-selects between the on-module buffer and the memory devices.

The Institution Decision notes that

Petitioner argues that it “would have been obvious to a [person of ordinary skill in the art] in light of JESD79-2 and knowledge of the JEDEC standards that the memory controller would provide multiple chip-select signals to the memory module,” citing in support JEDEC DIMM standards that show pins for receiving chip select signals at the memory module. Paper 11 at 19.

Again, “JEDEC DIMM standards” is not part of the grounds. The Board’s remark also presumes that a POSITA would have applied JEDEC-style design to Perego’s non-JEDEC compliant design. Perego’s entire design is focused on avoiding the need for off-module chip select signals: that is why it never mentions that signal. Indeed, even when Perego describes that there may be individual control and address RQ lines, it does not mention chip-select as well as CKE, WE, or other signals characteristic of JEDEC-compliant DIMMs. *See, e.g.*, EX1071, 9:58-60. On the full trial record there is no motivation to combine.

The Petition suffers many additional deficiencies, including the failure to

overcome the examiner’s prior finding that the art of record—including substantially the same references at issue here—did not disclose the limitations related to the claimed memory module’s CAS latency. EX1002, 229. But the Petition’s lack of disclosure or motivation to implement the claimed input chip-select signals is independently fatal to every asserted ground.

Petitioner additionally relies on Ellsberry and Halbert, but Ellsberry is neither prior art to the ’417 Patent nor qualifies as a patent or printed publication under § 311(b), and while Halbert appears to disclose multiple “ranks,” it explains that “all of multiple ranks will receive the same address and commands,” EX1078, 4:57-59, which means it effectively includes only a single rank and thus does not disclose “a plurality of N-bit wide ranks” receiving chip-select signals with different values as required by each claim of the ’417 Patent.

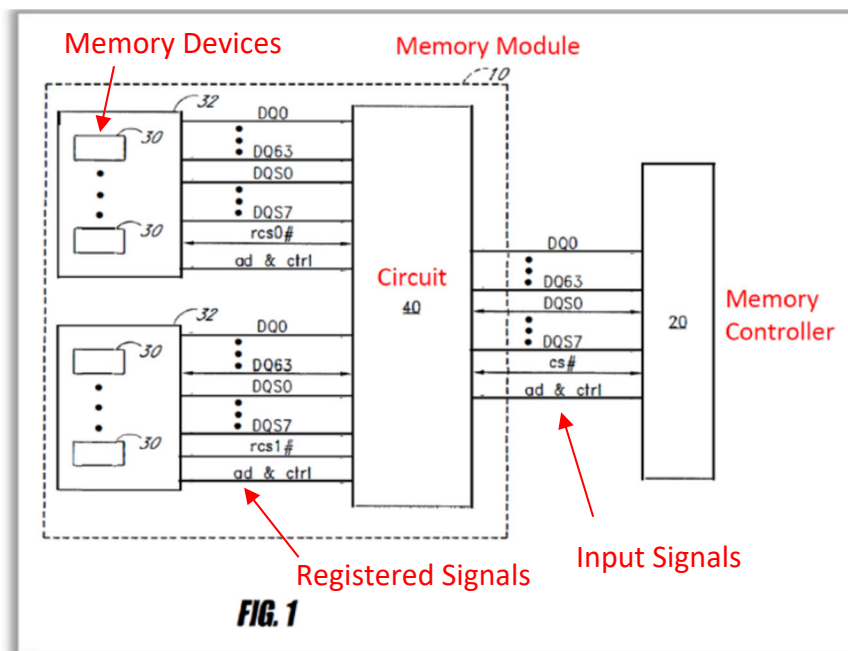
Consequently, the Board should find that Petitioner has failed to demonstrate the obviousness of the challenged claims.

II. THE ’417 PATENT

The ’417 Patent (EX1001), titled “Memory Module With Data Buffering,” relates to a memory module that effects “registered transfers of N-bit wide data signals with [a] memory read or write command between [a] N-bit wide memory bus and ... memory devices in response to ... data buffer control signals and in accordance with an overall CAS latency of the memory module, which is greater

than an actual operational CAS latency of the memory devices.” EX1001, Abstract. The data buffer control signals are output by a logic on the module, which is “configurable to receive a set of input address and control signals associated with [the] read or write memory command and output registered address and control signals [in addition to] data buffer control signals.” *Id.*

Figure 1, annotated below, illustrates such a module. EX1001, 5:65-67.



As shown, “[t]he memory module 10 is connectable to a memory controller 20.” *Id.*, 5:67-6:1. In the Figure 1 example, the memory module 10 includes multiple memory devices 30 arranged in two ranks 32, each rank having multiple memory devices 30. *Id.*, Fig. 1, 7:11-13.

The memory module 10 also includes a circuit 40 electrically coupled to the memory devices 30 and to the memory controller 20 of the computer system. *Id.*,

6:4-7. The circuit 40 includes logic that translates between a system memory domain of the computer system and a physical memory domain of the memory module 10. *Id.*, 6:9-12. This may be achieved by the logic receiving input data signals, chip-select signals and other control/address signals from the memory controller 20, and outputting corresponding registered data signals, registered chip-select signals and other registered control/address signals to the memory devices 30. *See* EX1001, Fig. 1, 21:66-22:35; *see also id.*, 18:37-19:9 (showing how the logic translates the input control/address and chip-select signals).

The memory module also includes an SPD device 240 that can report the CAS latency (CL) of the memory module to the memory controller 20. *Id.*, 22:36-38. The reported CL value of the memory module may be “one more cycle than does the actual operational CL of the memory array,” for example to account for the fact that in some embodiments, “data transfers between the memory controller 20 and the memory module are registered for one additional clock cycle by the circuit 40.” *Id.*, 22:38-43.

III. SKILL LEVEL OF A POSITA

For purposes of this Response, Netlist applies the skill level proposed by Petitioner with one modification. As explained by Dr. Przybylski, the design of memory module and memory devices are two distinct fields. EX2024, ¶ 68. Accordingly, while Petitioner suggests, in part, that a POSITA would have been

“knowledgeable about the design and operation of standardized DRAM and SDRAM memory devices and memory modules and how they interacted with the memory controller of a computer system” (Pet. 9), in Netlist’s view a POSITA would have been “knowledgeable about the operation of standardized DRAM and SDRAM memory devices and memory modules including these commercially available devices.” EX2024, ¶ 68.

IV. CLAIM CONSTRUCTION

Netlist disagrees with Petitioner’s proposed construction for “rank,” in particular, that a rank could include a single memory device. *Contra* Pet. 26. However, the Board need not resolve that dispute to address the parties’ arguments regarding the challenged claims. Netlist notes that the parties’ submitted competing constructions of terms including “rank” in the related district-court proceeding, and the court recently issued a construction: “a ‘bank’ of one or more devices on a memory module that operate in response to a given signal.” EX2030, 12-15. Netlist disagrees with that construction due to the use of the undefined and ambiguous term “bank” and the lack of clarity regarding what it means to “operate in response to a given signal,” as well as the construction’s inconsistency with the plain and ordinary meaning of the term as reflected, for example, in JEDEC standards documents, *see, e.g.*, EX2031 (JESD21-C SPD Standard), 7 (“Rank: any DRAMs connected to the same physical CS [chip select pins]”); EX2024, ¶¶ 62-65, as well as Dr. Wolfe’s

description of “rank” as including memory devices that “are acting together in response to the chip select signals, to read or write the full bit width of the memory module.” EX2033 (Wolfe Deposition Transcript), 154:7-24.

Solely for purposes of responding to this Petition, however, Netlist applies Petitioner’s proposed construction: “an independent set of one or more memory devices on a memory module that act together in response to command signals, including chip-select signals, to read or write the full bit-width of the memory module.” Pet. 26; *cf. SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1355 (2018) (“[I]n an inter partes review the petitioner is master of its complaint....”).

V. ASSERTED PRIOR ART

A. Perego

Perego (EX1071) discloses a memory system with a Rambus-style point-to-point topology including a “memory module having a buffer device (e.g., having a configurable width) isolating data, control, and address signals of the memory devices from the connector interface.” EX1071, 4:38-45, Abstract, 5:35-55, 8:10-17, 8:20-26. Buffer device 350 is coupled to memory controller interface 375, which includes a “plurality of memory subsystem ports 378a-378n.” *Id.*, 4:63-5:15. Perego’s configurable width buffer device is connected to ports 378a-378n of the memory controller via a point-to-point links 320. *Id.*, 5:12-21. Perego repeatedly and consistently emphasizes the benefits of its point-to-point architecture over a

conventional JEDEC-style bus. *See, e.g.*, 3:47-56, 4:65-5:1, 5:6-15, 5:32-55, 6:15-19, 13:49-59, 21:46-50, Figs. 3A/3B, Fig. 5A.

Perego's buffer communicates to the plurality of memory devices on the buffered module via channels 370. *Id.*, 5:4-6, 6:13-24, 7:65-67, Fig. 3B. But in contrast to a conventional registered DIMM ("RDIMM"), in Perego's architecture, control/address information is transmitted to the module via packets and multiplexed with data in order to be transmitted via the point-to-point links. *Id.*, 13:49-59 (configurable width interface 590 may "extract the address and control information from the data"). In the example of a "normal memory read operation," Perego explains that "device 350 receives control, and address *information* from controller 310 via point-to-point link 320a, and *in response, transmits corresponding signals to one or more, or all of memory devices 360* via channels 370," *id.*, 6:12-19, but the same paragraph contrasts this approach with that of the conventional RDIMM buffer. *See id.*, 6:27-30 ("By way of comparison, buffers disposed on the conventional DIMM module in U.S. Pat. No. 5,513,135 are employed to buffer or register control signals such as RAS, and CAS, etc., and address signals."); Pet. 32-33 (arguing that the '135 Patent (EX1081) is an example of a JEDEC-compliant RDIMM that Perego allegedly would make upgradeable with its invention).

Perego discloses that regardless of the module width, "[a] module's full set of

data stored on the associated memory devices is available[.]” EX1071, 7:54-56. “With wider interface widths, different subsets of memory devices and memory cells may be accessed through different sets of interface connections. With narrower data or interface widths, the different subsets of memory devices and memory cells are accessed through a common set of interface connections.” *Id.*, 7:56-62. Address bits are used to specify the memory devices to be accessed at narrower interface width. *Id.*, 7:62-64.

Perego specifically refers to a dynamic point-to-point topology to connect the memory controller to the memory subsystem/module. EX1071, 3:41-47, 5:32-55, 6:57-7:29. A POSITA would recognize this terminology as being specific to the Rambus XDR architecture. EX2024, ¶ 96; EX1071, 8:1-9, EX2009, 10-12, 15, 17.

The embodiments of Figure 5A and 5B show the connections between the point-to-point link (or primary channel). EX1071, 15:7-13. Each include one or more interfaces 520. *Id.*, 16:20-21. The interfaces “receive and transmit to memory devices to memory devices disposed on the module (*see, e.g.*, FIGS. 4A, 4B and 4C) via channels.” *Id.*, 11:48-51. These are the channels 415 of Figures 4A-4C, which a POSITA would recognize as Direct RDRAM channels. EX2024, ¶ 100; EX1071, Figs. 4A, 4B, 4C; EX2026, 8. Perego describes that the interfaces 520 can include any number of channels. EX1071, 11:51-55.

The embodiments Figure 4A-4C utilize the buffer device 405, shown in Figure 5A. This buffer device, like the configurable width buffer device shown in Figure 5B, has a singular request and address logic block 540 which receives control and address information from the interface 510/590. EX1071, 13:54-59. Depending on the bandwidth of the interface 510 of Figure 5A, both interfaces 520a and 520b are combined to respond to a memory access request. *Id.*, 11:56-12:2. Thus interfaces are two halves of one singular memory interface that, depending on the present configuration, may be used only partially used. Further details are found in EX2034, a patent that issued from U.S. Patent Application No. 09/797,099, which is incorporated by reference into Perego. EX1071, 7:9-17; *see* EX2024, ¶¶ 102-07.

Perego discloses that memory devices 410a-410h in the embodiments of Figures 4A-4C are Rambus DRAMs. EX1071, 10:54-56. The linear channels in which control and data components travel in parallel to all the memory devices in the channel is a characteristic of Direct RDRAM channels. *Id.*, Figs. 4A, 4B, 4C, 9:43-45; EX2026, Fig. 3; EX2025, 46-47; *see* EX2024, ¶¶ 108-09.

B. JESD79-2

JESD79-2 (EX1064) is the first version of the JEDEC standard for DDR2 SDRAMs. JESD79-2 is a memory *device* standard, not a memory *module* standard. Accordingly, it does not define the memory bus or signals it carries between a module and an external memory controller or any other characteristics or features of

other devices on the module, such as buffers or registers. Petitioner frequently cites versions of JESD21-C, which is a JEDEC standard for modules, such as DDR RDIMMs (EX1062) and DDR2 RDIMMs (EX1066), but they are distinct standards and are not part of the JESD79-2 reference identified in Petitioner's grounds.

C. Ellsberry

Ellsberry (EX1073) discloses a memory module architecture that “permits transparent bank switching of memory devices.” EX1073, [0001]. As depicted in Figure 2, Control ASIC 204 “receives memory addresses and commands over the DIMM interface 202” from the system memory controller, and switch ASICs 206 and 208 “receive data information from the DIMM interface 202 via data buses 230 & 232, respectively.” *Id.*, [0028]-[0029]. Each switch ASIC is connected to a number of memory banks (e.g., Bank 0-3 below). *Id.*

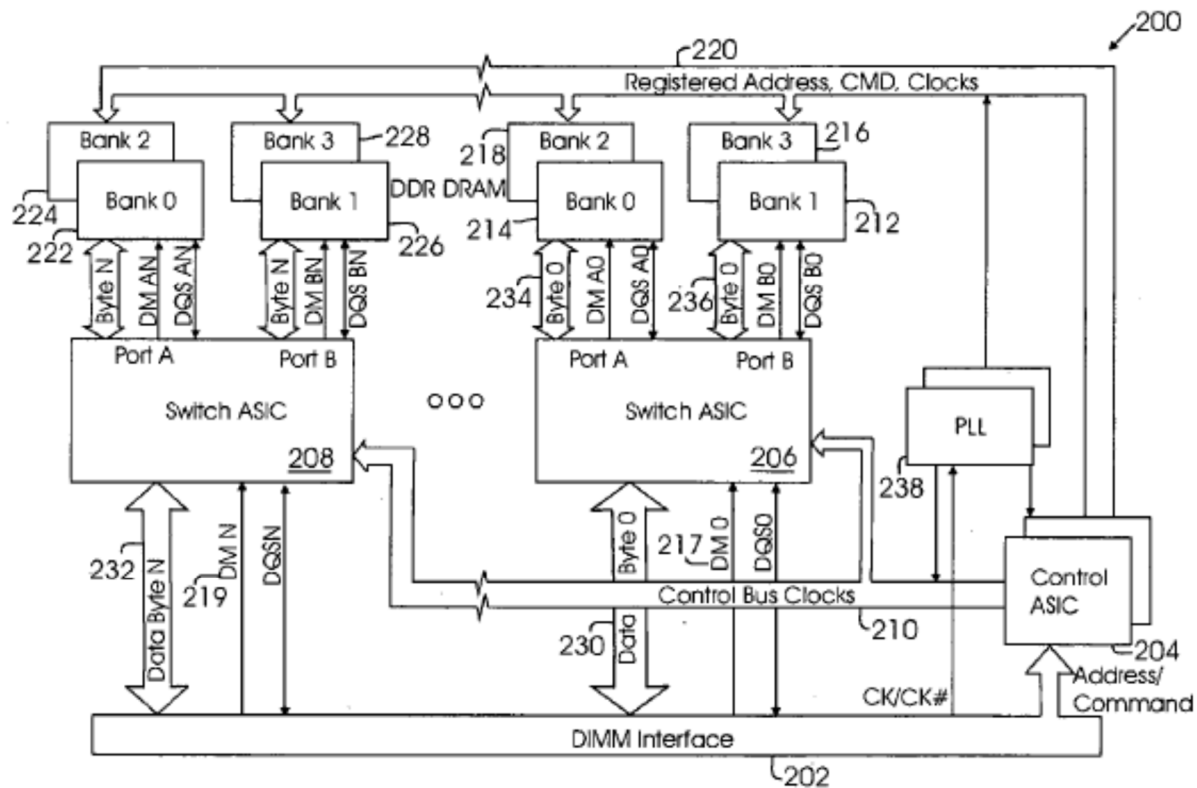


Fig. 2

EX1073, Fig. 2. Switch ASICs 206 and 208 receive respectively data byte group N and data byte group 0, provided “simultaneously” by the DIMM interface 202. *Id.*, [0030], Fig. 2 (depicting at least two data groups); Fig. 5 (depicting nine).

Control ASIC 204 sends command signals to memory devices in different memory banks via bus 220. *Id.*, [0030]. This includes mode register set (MRS) commands that sets the CAS latency (CL). *See*, Fig. 8A for commands. MRS is not sent to the ASIC switches. *See* EX1073 *generally*. Each ASIC switch includes two data ports, Port A and Port B, coupled respectively to data busses 234 and 236. Ellsberry discloses that in column addressing scheme, memory devices coupled to

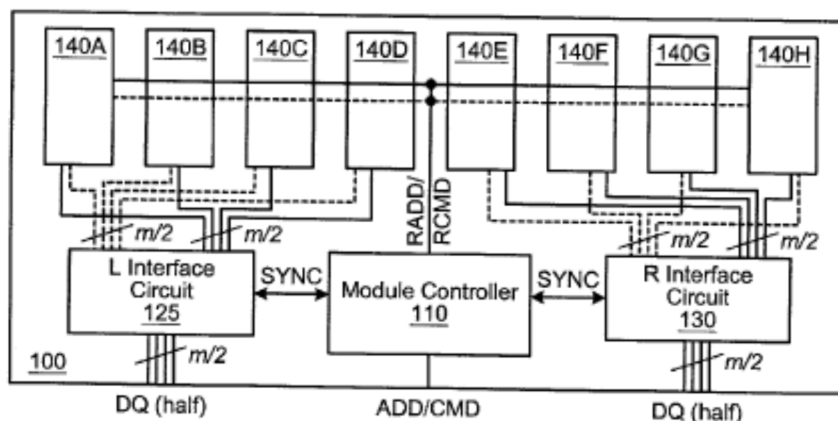
both ports A and B are read but only the data from the target memory device is multiplexed onto the DIMM interface. EX1073, [0033].

D. Halbert

Halbert (EX1078) generally discloses memory module architectures and methods for operating a memory module. EX1078, 1:16-19. As shown in Figures 1 and 8, bus 22 is arranged with a backbone of address, command, and data signal lines, which provide an electrical connection for data exchange between memory controller 20 and memory modules 100A-C. *Id.*, 1:31-39, 1:61-2:14, Figs. 1, 8. Figure 8 of Halbert also shows what it describes as a first “rank” of memory devices 140A-H on one side of the module, and a second “rank” of memory devices 142A-H arranged on the back side of the module. *Id.*, 7:31-53.

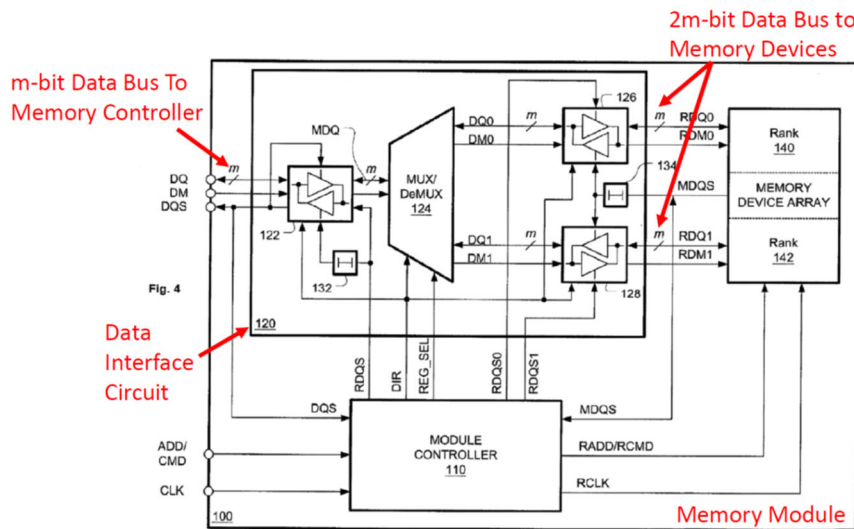
Figure 7 of Halbert illustrates first m-bit wide data lines (solid lines) connected to the first rank 140A-H on the front side, and second m-bit wide data lines (dashed lines) connected to the second rank 142A-H on the back side.

Fig. 7



EX1078, Fig. 7. As shown above, the Halbert device includes module controller 110, which receives addresses and commands from a memory controller and sends those addresses and commands to memory devices 140A-H. *Id.* Figure 7 also includes two data interface circuits 125 and 130. *Id.*

Petitioner relies upon Halbert's Figure 4 embodiment (*see, e.g.,* Pet. 127), which shows the schematic representation of memory module 100 including just one interface circuit 120 and some of its internal structure.



EX1078, Figure 4 (annotated). Memory module 100 includes module controller 110, data interface 120, and memory devices in ranks 140 and 142. Data interface 120 is coupled on the left side to the system memory controller via m-bit wide system memory data bus (DQ) and on the right side to two ranks 140 and 142 of memory devices via a 2m-bit wide module data bus (comprising two parallel m-bit wide module data buses RDQ0 coupled to rank 140 and RDQ1 coupled to rank 142). Each

of the ranks 140 and 142 comprises a plurality of memory devices or a device array. EX1078, Figure 8, 4:36-5:22, 7:31-53. Module controller 110 controls the operation of data interface circuit 120 by “providing timing and synchronization signals to data interface circuit 120.” *Id.*, 4:40-48. Module controller 110 also provides command, address, strobe and clock signals to the memory devices in ranks 140 and 142 (*see* buses RADD/RCMD and signals RCLK).

Halbert teaches using the data interface circuit 120 to aggregate data transfers between “slower memory devices” (e.g., memory devices in ranks 140 and 142) and a “faster system memory bus,” by accessing the multiple ranks of memory devices 140 and 142 simultaneously and in parallel. The data interface circuit 120 interfaces with “slower memory devices” via a wider (2m-bit) module data bus at half the data rate of the narrower (m-bit) and “faster system memory bus.” *Id.*, 4:36-5:22. In this manner, “*multiple ranks will receive the same address and commands*, and will *perform memory operations with the interface circuit concurrently.*” *Id.*, 4:57-59. According to Halbert, this design “widens the data bus on the memory module as compared to the width of the system memory data bus,” which “allow[s] a faster system memory data bus to operate at full speed with slower memory devices.” *Id.*, 3:43-48. In other words, the memory device array has a data interface twice as wide and half the data rate as the memory bus between the module and memory controller.

VI. PETITIONER HAS NOT ESTABLISHED OBVIOUSNESS UNDER GROUND 1

Petitioner's proposed combination of Perego and JESD79-2 would not render the claimed invention of the '417 Patent obvious because it fails to disclose key limitations of the challenged claims and would not have motivated a POSITA to alter Perego's memory modules as Petitioner suggests.

Perego fails to disclose a plurality of N-bit wide ranks, input chip-select signals, corresponding registered chip-select signals, and other claimed limitations specific to JEDEC-standardized memory modules, and instead discloses a Rambus memory module architecture that is fundamentally incompatible with a traditional JEDEC DIMM. At Institution, the Board observed that "Perego discloses using DDR2 memory devices." Paper 11 at 14. While JESD79-2 may inform a POSITA regarding how to interface DDR2 SDRAMs with Perego's buffer, JESD79-2 would not suggest modifying Perego's Rambus module to implement, for example, the claimed "input chip-select signals." The Institution Decision notes that "Patent Owner focuses on the lack of a chip select network, which is not recited in the claims of the '417 patent." Paper 11, at 14. The claims recite "input-chip select signals" from the off-module memory controllers. Perego does not implement this type of design, it has a lack of a chip select network. JESD79-2 does not disclose chip selects from the off-module memory controller to the module. It focuses solely on chip

select signals between an on-module buffer and the chips. The Institution Decision notes that

Petitioner argues that it “would have been obvious to a [person of ordinary skill in the art] in light of JESD79-2 and knowledge of the JEDEC standards that the memory controller would provide multiple chip-select signals to the memory module,” citing in support JEDEC DIMM standards that show pins for receiving chip select signals at the memory module. Paper 11, at 19

Internal chip select signals on a module are not the same as the chip select signals coming from an off-module controller onto the module. Perego’s entire design is focused on avoiding the need for off-module chip select signals. On the full trial record there is no motivation to combine.

A. A POSITA Would Not Have Combined Perego and JESD79-2 in the Manner Contemplated by Petitioner

Petitioner contends that a POSITA would have been motivated to combine the teachings of Perego and JESD79-2 because Perego discloses that its memory modules can use DDR2 memory devices, and the JEDEC standard for DDR2 SDRAMs is JESD79-2. Pet. 30. More specifically, Petitioner argues that “[a] POSITA would have ... been motivated to implement Perego’s memory modules in a registered DIMM format with DDR memory devices that fits into DIMM

connectors and uses DIMM module input signals, according to JEDEC standards, including JESD21-C and JESD79-2.” Pet. 32.

In other words, Petitioner contends that a POSITA would not only look to JESD79-2 to incorporate DDR2 SDRAMs into Perego on one side of the buffer, but also to JESD21-C (the JEDEC DDR2 RDIMM standard) to replace Perego’s high-performance “memory system architecture and topology centered around a dynamic point-to-point interconnect connecting the memory controller to the memory subsystems/modules” on the other side of the buffer (EX2024, ¶ 128; EX1071, 2:40-42, 4:64-5:15), with a traditional RDIMM bus. This proposal poses several problems not addressed by Petitioner.

1. JESD79-2 Is a DDR2 Memory Device Standard, Not a JEDEC Memory Module Standard

First, neither Perego nor JESD79-2 is directed to JEDEC-standardized memory modules, such as DDR2 RDIMMs. Rather, Perego “explicitly turns away from that style of memory system architecture to develop systems that are both higher performance and expandable and which different embodiments can use different memory types without changing the primary channel characteristics or the advantages of its memory system architecture,” EX2024, ¶ 144; EX1071, 4:63-5:15, and JESD79-2 (EX1062) is one version of the JEDEC standard for memory *devices* (such as DDR SDRAMs), not memory *modules* (such as DDR2 RDIMMs). EX2033

(Wolfe Deposition Transcript), 105:4-5 (“1064 is just a device specification. It’s not the module specification.”). This distinction is important because the ’417 Patent claims require an “N-bit wide memory bus,” “address and control signal lines and data signal lines” in the memory bus, “logic,” “circuitry,” and “N-bit wide ranks” (EX1071, 42:7-67), among other components that are distinct from individual memory devices but comport with components on JEDEC-standardized modules. EX2024, ¶ 144.

2. Perego’s Rambus Modules Are Fundamentally Different than the RDIMMs Defined in JESD21-C

Second, Petitioner’s own evidence reveals the vast differences between JEDEC and Rambus module architectures. *See* EX1069, 11-16 (discussing the differences between JEDEC-style memory and Rambus memory). This is particularly true for chip-select signals, which are a hallmark of JEDEC-compliant bus architecture and relate to several claim elements of the ’417 Patent. *E.g.*, EX2024, ¶ 129; EX1069, 2 (characterizing “the chip-select bus” as “essential in a JEDEC-style memory system”). The Board observed that Petitioner does not even argue that Perego discloses (input) chip-select signals from off-module. Paper 11, 18. For good reason. Chip-select signals are used to select ranks, *e.g.*, EX2031, 7 (“Rank: any DRAMs connected to the same CS”)), and the concept of ranks is foreign to Rambus systems like Perego that can address each memory device

individually. *E.g.*, EX2009, 16 (rather than addressing a rank, the memory controller addresses a single device in Rambus XDR architecture); EX2001, 20-24 (contrasting Rambus Direct topology in which “a Direct RDRAM spans the entire channel” so that the “CPU accesses each RDRAM independently” with traditional DRAM systems in which “several conventional DRAMs [i.e., a rank of memory devices] are frequently ganged together in parallel to provide the necessary aggregate bandwidth”). Even when Perego discusses providing “individual control lines,” it never mentions a chip-select signal line (or any of the other signal lines characteristic of a JEDEC-style RDIMM, such as CKE, DQS, etc.). *See, e.g.*, EX1071, 9:58-60; EX2024, ¶ 129 (describing required elements of JESD21-C (citing EX1066, 6)); EX1069, 12 (contrasting Rambus protocol with traditional JEDEC-style protocol, including the absence of chip-select networks in Rambus memory organization); EX2002 (no chip select input for RIMMs); EX2001, 20-23 (no chip select signals mentioned for Rambus Direct); EX2024, ¶¶ 129, 139.

Good reason exists for why the disclosure omits those characteristics input control signals needed for JEDEC-style DIMMs. For example, JESD21-C (RDIMM Standard) requires clock enables, chip selects, exactly three bank address signals, on-die termination (ODT), bidirectional differential data strobe signals, data mask signals and a voltage reference signal (EX1066, 6), each of which would be “unnecessary, unusable or detrimental in the context of Perego’s memory system

and module architecture.” EX2024, ¶ 129 (citing, for example, additional bank address bits necessary for Direct RDRAM and XDR DRAMs), 139. Furthermore, the RDIMM relied on by Petitioners has a fixed buffer width (EX2003, 43:12-20; EX1064, 1-6, EX2024, ¶ 24), whereas configurable width buffer devices are central to Perego. *E.g.*, EX1071, Abstract, Title, Figs. 3C, 4A, 5A, 5B, 13:6-17, 13:49-59, 14:52-15:6, 15:31-45, 17:22-33. And this configurable data bus width influences Perego’s addressing structure. EX2024, ¶ 130. Indeed, according to Dr. Przybylski, a chip-select-based addressing scheme would not be compatible with Perego’s variable width interfaces. EX2024, ¶ 135; EX1071, 16:66-17:8; *see also* EX2024, ¶ 190 (noting that Perego focuses on “a dynamic point-to-point memory system topology and configurable data path widths allowing for changes to the capacity of the memory system, changing the number of used DQ signal traces on the primary channel without losing access to any of the storage locations”).

In sum, JEDEC-complaint, chip-select-dependent RDIMM architecture defined in JESD21-C is fundamentally at odds with the Rambus point-to-point topology and variable bit width interfaces of Perego. While Perego states a goal of “retaining backward compatibility with existing generations of memory *devices*” (EX1071, 6:37-39), that does not imply backward compatibility with existing memory *modules*, such as RDIMMs. In fact, Perego contrasts its memory modules with “conventional DIMM module designs,” EX1071, 6:27-33; *see also id.* 1:31-49

(“conventional memory system” of Fig. 1), 2:15-30 (“need for memory system architectures or interconnect topologies that provide flexible and cost effective upgrade capabilities while providing high bandwidth”). Indeed, a key benefit described by Perego is the ability to preserve not only backward compatibility for memory devices, but also “new generations of memory devices.” EX1071, 6:37-43. The high-performance Rambus-style primary channel of Perego facilitates this compatibility. EX2024, ¶ 134; EX1071, 8:1-5, 3:23-40. Implementing a traditional bus architecture would severely limit forward-facing compatibility.

3. The Petition Fails to Identify JESD21-C in Any Ground

Despite Petitioner’s heavy reliance on JEDEC memory module standards, the Petition identified only three Grounds, none of which includes a JESD21-C reference. *See* Pet. 5. Therefore, Petitioner should not be permitted to rely on EX1062 or EX1066 as though it had included them in the Grounds. “As the Supreme Court has stated, in an IPR ‘the petitioner’s contentions ... define the scope of the litigation all the way from institution through to conclusion.’” *Corephotonics, Ltd. v. Apple Inc.*, 84 F.4th 990, 1001 (Fed. Cir. 2023) (quoting *SAS Inst.*, 138 S. Ct. at 1357). Thus, the Petition “define[s] the contours of the proceeding,” *SAS Inst.*, 138 S. Ct. at 1355, and the Federal Circuit has held that “the Board erred by instituting inter partes review based on a combination of prior art references not advanced in [the] petition.” *Koninklijke Philips N.V. v. Google LLC*, 948 F.3d 1330, 1335 (Fed.

Cir. 2020); *see also* 37 C.F.R. § 42.104(b) (Petition must identify “[t]he specific statutory grounds ... on which the challenge to the claim is based and the patents or printed publications relied upon for each ground.”). While courts have permitted the Board to reference “the skilled artisan’s knowledge when determining whether it would have been obvious to modify the prior art,” *Koninklijke Philips*, 948 F.3d at 1337, here Petitioner’s necessary—if not always express—reliance on JESD21-C is pervasive and fundamental to its core contentions. Petitioner should have identified its Grounds accurately in the Petition and made the required showing of a motivation to combination with a reasonable expectation of success all three references. *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016) (“It is of the utmost importance that petitioners in the IPR proceedings adhere to the requirement that the initial petition identify “with particularity” the “evidence that supports the grounds for the challenge to each claim.” (quoting 35 U.S.C. § 312(a)(3))).

4. Perego Teaches a POSITA to Incorporate DDR2 SDRAMs Without Changing the Rambus Module Architecture

As noted above, Petitioner’s reliance on Perego’s statements regarding backward compatibility as a motivation to implement a JESD20-C bus in Perego is misplaced. One of Perego’s significant benefits is its flexibility to implement a wide variety of memory devices in the embodiment depicted in Figs. 4A-4C. EX1071,

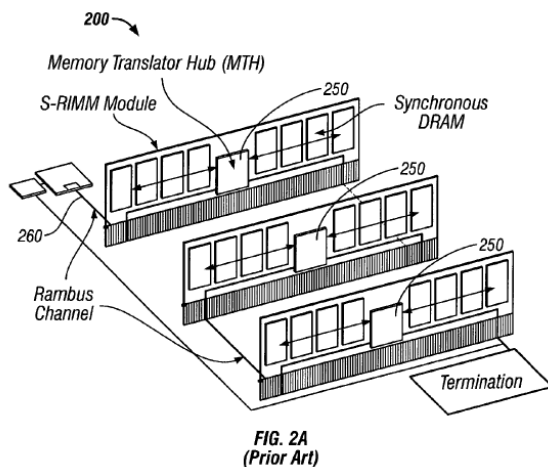
10:54-67 (“[d]ifferent types of memory devices may be included on different modules within a memory system by employing buffer device 405 to translate protocols employed by controller 310 to the protocol utilized in a particular memory device implementation,” which “may feasibly render the type of memory device transparent to the system”). As Dr. Przybylski explains, “this technique is directly illustrated in prior art figure 2A, in which JEDEC-compliant Synchronous DRAMs are used on an S-RIMM module the interface of which is compatible with the Rambus Direct RDRAM architecture.” EX2024, ¶ 133 (citing EX1071, Fig. 2A, 2:8-10). And as explained above, “the backward and forward compatibility is facilitated by having a high performance primary channel such as the point-to-point links disclosed.” EX2024, ¶ 134.

Tellingly, Petitioner does not acknowledge Perego’s disclosure of buffer-translation to accommodate DDR2 SDRAM devices. EX1071, 10:56-67. But that disclosure is central to how Perego achieves its goal of backward and forward compatibility; and Petitioner’s combination of Perego and JESD79-2 (DDR2 SDRAM Standard) would lead a POSITA to this choice in view of Perego’s express encouragement to leverage the buffer’s translation ability without needing to alter Perego’s primary channel interface or configurable bit-width flexibility. Given this existing superior solution, a POSITA would not be motivated to look to JESD21-C to revamp Perego’s module architecture (EX2024, ¶ 139), and Petitioner’s failure to

address this disclosure is fatal to Ground 1. Indeed, Petitioner fails to identify any concrete benefit that would result from downgrading Perego's module to something compatible with JESD21-C. *See Innogenetics, N.V. v. Abbott Lab'ys*, 512 F.3d 1363, 1374 (Fed. Cir. 2008) (affirming preclusion of "vague and conclusory obviousness testimony which did not offer any motivation for one skilled in the art to combine the particular references ... in order to practice the claimed method"); *id.* at 1374 n.3 ("We must still be careful not to allow hindsight reconstruction of references to reach the claimed invention without any explanation as to how or why the references would be combined to produce the claimed invention."). Petitioner here completely failed to articulate a plausible motivation to combine JESD79-2 and Perego in such a way as to arrive at the claimed invention of the '417 Patent in view of Perego's buffer translation functionality.

Petitioner may argue that "inferior" combinations would still render claims invalid, but the pertinent question is why a POSITA would have modified an existing design knowing that the resulting modification would be inferior. Petitioner has not presented any evidence that a POSITA, one of ordinary creativity, would have thought it would be desirable to do so. Nor has Petitioner presented any evidence such as "design incentives, [or] other market forces" to "prompt variations" of the Perego design. *KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1731 (2007).

As a matter of fact, even in Perego's "prior art" design cited by Petitioner, Perego does not give up his own proprietary primary-channel architecture when paired with JEDEC-standard SDRAMs. Instead, he uses an S-RIMM format with Rambus proprietary module memory bus architecture as shown in Figure 2A:



EX1071, Fig. 2A; EX2024, ¶ 112 ("Figure 2A of Perego shows exactly this type of memory system in which the memories are SDRAM and the primary channel is a Direct RDRAM channel." (citing EX1071, 2:8-10)), 113 (noting that the SDRAM devices in Figure 2A "receive chip select signals even though the Direct Rambus Channel on which the modules sit does not include any chip select signals" and that "a POSTA would understand that those CS signals to the SDRAMs were generated locally by the Memory Translator Hub (MTH) from the addressing information"). This would suggest to a POSITA the importance to Perego of retaining his primary bus architecture. See EX2024, ¶ 137 ("Changing the primary channel of Perego to

resemble that of a DDR2 SDRAM as suggested in the Petition would deprive Perego of the basis of its advantages....”).

5. Petitioner Fails to Explain Why a POSITA Would Sacrifice Perego’s Benefits and Alter Perego’s Basic Principles

Imposing a JEDEC-compatible bus in Perego’s memory system would pose significant logistical challenges not even acknowledged, much less addressed, by Petitioner. *See, e.g.*, EX2024, ¶¶ 134-40. Moreover, the Petition fails to identify a motivation to alter Perego so significantly and cripple several of the core functionalities described as benefits in the Perego patent. While the test for obviousness is not bodily incorporation, *e.g.*, *MCM Portfolio LLC v. Hewlett-Packard Co.*, 812 F.3d 1284, 1294 (Fed. Cir. 2015), where “the ‘suggested combination of references would require a substantial reconstruction and redesign of the elements shown’ in [one of them], or a ‘change in its basic principles’” under which it was designed to operate, that counsels against finding of obviousness. *Univ. of Md. Biotechnology Inst. v. Presens Precision Sensing GmbH*, 711 F. App’x 1007, 1011 (Fed. Cir. 2017) (quoting *In re Ratti*, 270 F.2d 810, 813 (CCPA 1959) (en banc)); *Plas-Pak Indus., Inc. v. Sulzer Mixpac AG*, 600 F. App’x 755, 759 (Fed. Cir. 2015) (“[A] change in a reference’s ‘principle of operation’ is unlikely to motivate a person of ordinary skill to pursue a combination with that reference.”). That is

particularly true because Perego teaches the POSITA how to use JEDEC-compliant SDRAMs without altering the primary channel as discussed above.

For example, Petitioner’s proposed combination would severely cripple Perego’s memory system and eviscerate the functionality underpinning its “Configurable Width Buffered Module” title. EX1071. It would also downgrade Perego’s primary channel such that it could not be used with certain Rambus memory devices, preserve future memory device compatibility, or leverage bandwidth concentration—all touted as benefits by Perego. EX2024, ¶ 134; EX1071, 8:1-5, 3:23-40, 11:56-12:3, 10:56-67. In short, it is difficult to conceive how or why a POSITA, balancing the limitations of JESD79-2 and JESD21-C against the flexibility and DDR2 SDRAM compatibility of Perego, would be motivated to modify Perego. EX2024, ¶ 140; *see Broadcom, Corp. v. Emulex Corp.*, 732 F.3d 1325, 1334 (Fed. Cir. 2013) (affirming non-obviousness where the prior art reference was a “self-contained” system that “accomplished its objective and provided no suggestion to broaden that objective”).

B. Perego and JESD79-2 Do Not Teach or Suggest the ’417 Patent’s Claimed JEDEC-Style Memory Module

As described below, even if combined, Perego and JESD79-2 fail to disclose several important claim limitations.

1. Neither Perego nor JESD79-2 Disclose Chip-Select Signals as Inputs to the Memory Module or Corresponding Registered Chip-Select Signals

Because Perego utilizes Rambus module interfaces, *see* Section V.A, *supra*, and because JESD79-2 relates to DDR2 SDRAM memory devices on the opposite side of the buffer from the module’s bus or primary channel, it is no surprise that neither reference discloses the ’417 Patent’s claimed “plurality of input chip select signals” [1.c.2] or the “plurality of registered chip select signals corresponding to respective ones of the plurality of input chip select signals” [1.c.3]. See EX2033 (Wolfe Deposition Transcript), 150:9-14 (“Rambus protocols at that time did not include distinct chip select wires, as far as I know.”).

The Board preliminarily relied on a disclosure indicating that “chip-select information” is used in the “Rambus bus organization.” Paper 11 at 14 (quoting EX1069, 11-12). But “chip-select information” as used by Jacobs in EX1069 is not germane to the chip-select signals or lines required by JEDEC standards and the ’417 Patent. EX2024, ¶ 47 (“Therefore, *there are no chip-select signals* as the term would be understood by a POSITA *in either the Direct RDRAM or the XDR RDRAM architectures*.”). As Dr. Przybylski explains, “[t]he passages quoted by the Board from Ex. 1069 (Paper 11, at 14-15) say that the original RDRAM includes chip-select information. *This is not accurate*. The original RDRAM being described in these paragraphs ... did not have any dedicated fields that a POSITA would consider

as chip-select information or chip-select signals.” EX2024, ¶ 47 (citing EX2029, 277).

Petitioner’s arguments for these claim elements assume the modifications necessary to implement a JEDEC-compatible bus on Perego’s memory module, *e.g.*, Pet. 48-50, which is not a reasonable assumption for the numerous reasons explained above. *See* Section VI.A, *supra*. To the extent that Petitioner contends that Perego’s embodiments can natively support chip-select signals as module inputs, *see, e.g.*, Pet. 36 (asserting that Perego’s module “is compatible with prior-art computers using a traditional bus for data, address, and control signals consistent with the JEDEC standards”), 38 (“A POSITA would have understood that a data width of $W_{DP}=64$ corresponds to the 64-bit data width of a JEDEC-compliant registered DIMM module.”), Petitioner is incorrect. Even in Perego’s embodiments implementing bus lines, *see* Pet. 41 (citing EX1071, 9:58-60, Figs. 4A, 4B), a POSITA would understand that the primary channel’s inclusion of RQ, DQ, CTM, and CFM signal lines identifies a Direct RDRAM channel and *not* a JEDEC-compatible bus that includes ranks of memory devices and “input chip select signals” as required by the ’417 Patent. EX2024, ¶ 150. And again, disclosing input chip-select signals requires resort to JESD21-C, which is not part of Ground 1.

2. Perego Does Not Disclose “a Plurality of N-Bit Wide Ranks” Receiving Chip-Select Signals with Different Values

Perego does not use the word “rank,” *see generally* EX1071, much less disclose “a plurality of N-bit wide ranks” as required by the ’417 Patent, [1.d.1]. As noted above, Patent Owner applies Petitioner’s proposed claim construction of “rank” for purposes of this proceeding without conceding its correctness. *See* Section IV, *supra*; Pet. 26 (construing “rank” as “an independent set of one or more memory devices on a memory module that act together in response to command signals, including chip-select signals, to read or write the full bit-width of the memory module”). Perego does not disclose such “ranks,” particularly because Petitioner’s construction requires chip-select signals. EX2024, ¶¶ 162-75.

Petitioner nonetheless presents colored versions of Perego’s Figures 3C, 4A, 4B, and 4C to suggest ranks. Pet. 64-65. A POSITA, however, would understand that the memories depicted in Figures 4A-4C are Direct RDRAM embodiments, which do not receive chip-select signals. EX2024, ¶¶ 167, 170; EX1071, 10:54-56; *see also* discussion on pages 31-33 above. More generally, Rambus memory devices are incompatible with the concept of ranks because they are each accessed individually and thus do not “act together” as proposed by Petitioner. EX2001, 23 (“Because a Direct RDRAM spans the entire channel, the CPU accesses each

RDRAM independently. So each RDRAM directly adds to the number of memory banks accessible to the memory controller.”).

As for Figure 3C, Dr. Przybylski explains that Figure 3C does not indicate the type of DRAMs and could be used with DDR2 SDRAMs using the protocol translation function of Perego’s buffer. EX2024, ¶ 171; EX1071, 2:43-45, 7:30-39, 7:65-8:5, 13:6-17. In that configuration, Dr. Przybylski further explains that a POSITA would understand, particularly in view of the ’099 Application incorporated by reference in Perego, that interfaces 520a and 520b of the configurable buffer device 391 in Figure 3C work in tandem and that all of the memory devices would need to be activated together as one DDR SDRAM rank. EX2024, ¶ 172. This is because the devices would not know ahead of time whether all the devices would be invoked for a particular read/write transaction, so they would all need to be activated and be ready for operation. This differs from a JEDEC-style module, where only one rank at a time would be selected for a read or write operation.

Of course, a singular rank does not disclose a “plurality of N-bit wide ranks” [1d.1], nor could a “plurality of N-bit wide ranks correspond to respective ones of the plurality of registered chip select signals” [1.d.2]. And with a single rank, there would also be no need for the logic to receive a plurality of chip select signals with

different values even if a POSITA would have modified Perego's primary channel architecture to include chip select lines.

Moreover, it is not clear that any such rank would "read or write the full bit-width of the memory module" as required by Petitioner's construction. *See* EX2024, ¶¶ 173-75. In any event, no such "ranks" would receive "registered chip select signals corresponding to respective ones of the plurality of input chip select signals" [1.c.3] for the reasons discussed in Section VI.B.1, *supra*.

Petitioner also contends that Perego discloses ranks by describing "grouping memory devices into multiple independent target subsets (i.e. more independent banks)." Pet. 67 (quoting EX1071, 15:37-45); EX2033 (Wolfe Deposition Transcript), 71:5-72:4 (same). But as confirmed by Dr. Przybylski, this passage has nothing to do with ranks, much less ranks according to Petitioner's proposed construction, as it lacks disclosure of at least chip-select signals and "read[ing] or writ[ing] the full bit-width of the memory module" as required under Petitioner's construction. EX2024, ¶ 165. Indeed, Petitioner's own expert, Dr. Wolfe, testified to the opposite conclusion while testifying in IPR2022-00615 regarding a related Netlist patent. EX2003, 202:8-204:10 ("I do not think that this paragraph [Perego 15:37-45] specifies how ranks are selected or enabled," and "independent banks" refers to "the number of page registers which can be activated corresponding to different addresses" "throughout the system"). Furthermore, this paragraph of

Perego states that “the target subset of secondary channel lines may be selected via address bits,” EX1071, 15:37-40, which are distinct from the chip-select signals required by Petitioner’s construction.

C. Perego and JESD79-2 Do Not Disclose [1.f] Related to Data Transfer Delays and CAS Latency

As previously detailed (Paper 6, 60-61), the same or substantially the same references were before the examiner when he issued the Notice of Allowability and stated that the closest prior art failed to teach element [1.f]. EX1002, 229-30. This limitation requires “wherein data transfers through the circuitry are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.” EX1001, 42:63-67. Thus, [1.f] expressly requires data transfers to be registered through the claimed circuitry between the memory devices and the module bus. The claimed time delay must include delay in the data path; delay on the address/control path alone cannot satisfy this element. EX2024, ¶ 179.

Petitioner misleadingly contends that JEDEC standards teach adding “an additional clock cycle ... to the CAS latency of the memory devices to leave enough time for the register on the memory module to perform its functions.” Pet. 95. Petitioner cites two JEDEC standards that do not disclose element [1.f].

First, Petitioner invokes the DDR RDIMM Standard: “In a registered DIMM, data is delayed an additional clock cycle due to the on-DIMM pipeline register.” EX1062, 68 n.1. Setting aside the fact that this is another example of relying on a JEDEC *module* standard outside the identified Ground, and that no similar language is found in the DDR2 RDIMM Standards (*see* EX1066, 94-96), this reference does not disclose that “data transfers through the circuitry are registered” for any amount of delay. Indeed, the JEDEC-compliant RDIMMs defined in JESD21-C include no “circuitry” between the memory devices and the module inputs by which data could be registered. *See* EX1066, 9; EX2024, ¶ 179; EX1071, 6:27-33. Instead, the cited quote relates to delay due to registering the address and command signals and is not relevant to this claim element. EX1062, 68; EX2024, ¶ 179. Moreover, the concept of using the additional clock cycle caused by delay through RCD for delaying data on the data path comes from the inventors (EX1001, 22:41-56), and it is improper to use inventors’ insight against them.

Second, Petitioner cites pages of EX1064 (JESD79-2) that relate to Additive Latency (AL). But there is a reason this concept is found in the DDR2 SDRAM standard. AL relates to the latency of the SDRAMs—i.e., a portion of the “actual operational CAS latency of each of the memory devices” and not any additional latency at the module level. EX2024, ¶ 180; EX1064, at 14 (Additive Latency programmed in memory device using EMRS command), 24 (disclosing “RL = (AL

+ CL)” and that “[t]he command is held for the time of the Additive Latency (AL) before it is issued inside the device”); *see also* Paper 11, at 35 (“[T]o the extent the JESD79-2’s disclosure of AL is specific to the memory devices themselves, it would appear that this AL would impact the actual operational CAS latency of the memory device.”). Accordingly, even if Perego were adapted to be JEDEC-complaint, this element would be neither implemented nor obvious.

Petitioner also contends that Patent Owner is bound by a prior Board finding regarding a different Netlist patent reciting a different limitation regarding CAS latency. Pet. 93-94. That decision has no preclusive effect here, as the claim language at issue relates to “a latency value” and includes no limitations related to, for example, “data transfers through the circuitry [being] registered for an amount of time delay,” “the overall CAS latency of the module,” or “an actual operational CAS latency of each of the memory devices.” EX1001, [1.f]; EX1030 (Final Written Decision in IPR2017-00549), 3 (quoting relevant claim language: “wherein the first logic element is configured to determine a latency value based on a previous memory command received by the memory module from the memory controller, and wherein the first logic element controls the second logic element to selectively enable the data communication according to the latency value”). The previous claim, for example, imposes no requirement on the relative length between the overall CAS

latency of the module versus the actual operational CAS latency of each of the memory devices. Nor did the prior IPR involve the Perego reference.

Petitioner additionally relies on its expert Dr. Wolfe's assertion that "[it] would have been obvious to add one additional clock cycle to Perego ... so the 'circuitry' has enough time to perform its functions (including 'register[ing]' the data signals for interfaces 520a/b with latches 597f-m ...) using 'internal' clock circuit 570a-b" Pet. 95 (citing EX1003, ¶¶ 359-62; EX1071, Figs. 5B-5C). As Dr. Przybylski clarifies, however, there is no indication in Perego that the clock signals controlling these latches came from 570a-b. EX2024, ¶ 184. In addition to the portion of Perego relating to the latches in the multiplexer/demultiplexer circuit in Fig. 5C, Petitioner cites 18:65-19:3, which relates to a separate issue regarding whether the multiplexer/demultiplexer implements of full or partial crossbar. EX2024, ¶ 186. Finally, Petitioner cites EX1071, 12:65-13:5, which relates to "clock circuit 570a-b" and "adjusting internal clock signals with respect to an external clock." As explained by Dr. Przybylski, this disclosure is not relevant to whether or not delay is added to the data path through the buffer circuit, but rather to controlling phase alignment between clock signals to ensure incoming data capture. EX2024, ¶ 185; EX2035 (Direct Rambus Clock Generator), at 1-2, 8. Furthermore, Petitioner's speculation is also premised on alleged JEDEC compliance, which is refuted above.

VII. PETITIONER HAS NOT SHOWN OBVIOUSNESS UNDER GROUND 2

Ellsberry is not a “patent” or “printed publication” under § 311(b). Nor is it prior art to the ’417 Patent. Thus, Petitioner cannot rely on Ground 2 in challenging the patentability of the ’417 Patent. Moreover, Petitioner fails to provide a plausible motivation to combine Ellsberry’s teachings with Ground 1.

A. Ellsberry Is Neither a “Patent” nor a “Printed Publication” Under 35 U.S.C. § 311(b)

Section 311(b) limits prior-art assertions in IPR petitions to “patents or printed publications.” There is no dispute that Ellsberry is not a “patent,” but rather a published patent application. And Petitioner appears to agree that Ellsberry does not qualify as prior art as a “printed publication” based on its *actual* publication date. Pet. 5 (contending that the ’417 Patent’s claims lack support from any application filed before July 1, 2005); EX1073 (Ellsberry) (confirming June 1, 2005 filing date and December 7, 2006 publication date). Longstanding authority confirms that a reference qualifies as a “printed publication” under § 102(a) only when it is actually published—i.e., when it becomes “publicly accessible.” *Samsung Elecs. Co. v. Infobridge Pte.*, 929 F.3d 1363, 1368-69 (Fed. Cir. 2019).

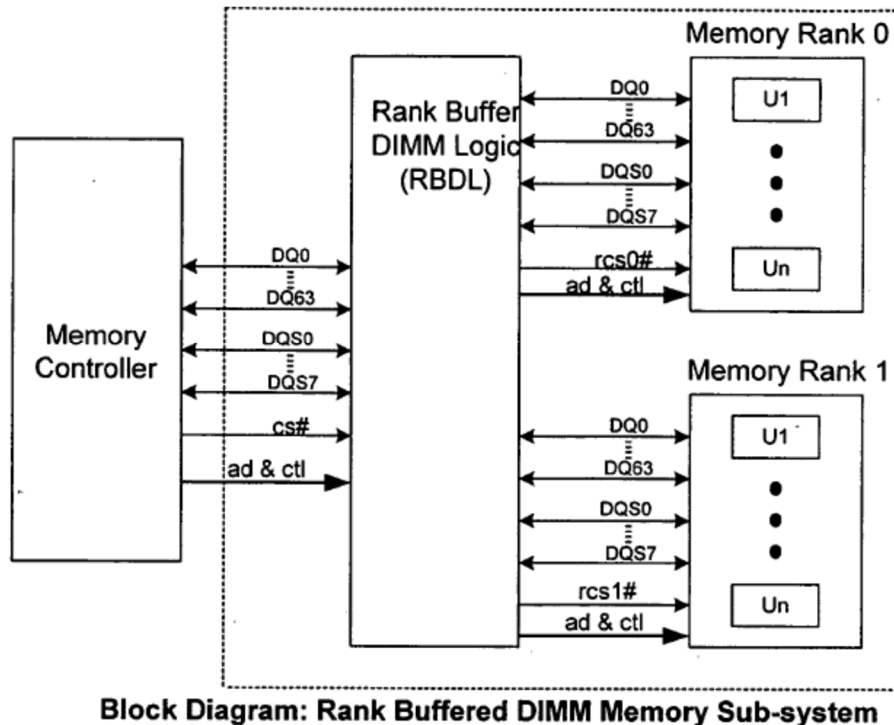
The Board preliminarily determined that Ellsberry nonetheless qualifies as a “printed publication” with the benefit of its June 2005 filing date because it was published (albeit not until December 2006) and because it qualifies as prior art under

pre-AIA § 102(e). Paper 11, 38-39. Netlist respectfully disagrees and is aware of no controlling precedent so holding. The fact that Ellsberry is “an application for patent, published under section 122(b) ... before [Petitioner’s alleged date of] the invention” as specified in pre-AIA § 102(e)(1) does not resolve the question. Indeed, not all prior art qualifies for use in IPR proceedings, and the term “printed publication” does not appear in that provision. If Ellsberry were a patent, it may qualify as prior art as of its filing date pursuant to pre-AIA § 102(e)(2) (addressing “a patent granted on an application”), but it is not. It is either a “printed publication” as of its December 2006 publication date or merely “an application for patent” that satisfies the terms of pre-AIA § 102(e) but was not included by Congress in § 311(b).

B. Ellsberry Is Not Prior Art to the '417 Patent

Even if Ellsberry qualifies under § 311(b) as of its filing date of June 1, 2005, it is not prior-art to the '417 Patent, which properly claims priority to, among other applications, U.S. Provisional Patent Application No. 60/588,244 (“the '087 Provisional”), which was filed prior to Ellsberry on January 19, 2005. EX1005, 2. Petitioner agrees that the '087 Provisional discloses “circuitry or ‘Buffer’ (RBDL) through which data (DQ0-DQ63) is communicated.” Pet. 6-7 (citing EX1005).

FIGURE 1:



EX1005, Fig. 1. Petitioner contends only that the '087 Provisional fails to disclose “data buffer control signals for enabling the transfer of data bursts through the buffer in response to read or write memory commands.” Pet. 7.

1. The '087 Provisional Provides Support for the Claimed Data Buffer Control Signals

Contrary to Petitioner’s assertion, the '087 Provisional provides adequate written description support for the limitations identified by Petitioner as allegedly absent in the January 2005 application. The absence of the specific words “data buffer control signals” is of no moment. The Federal Circuit has made clear that the specification need not recite the claimed invention verbatim. *Ariad Pharms., Inc. v.*

Eli Lilly & Co., 598 F.3d 1336, 1352 (Fed. Cir. 2010) (specification need not recite claimed invention *in haec verba*). Moreover, patent applications need not include and should omit that which is well known and accepted in the art. *LizardTech, Inc. v. Earth Res. Mapping, Inc.*, 424 F.3d 1336, 1345 (Fed. Cir. 2005) (“[T]he patent specification is written for a [POSITA], and such a person comes to the patent with the knowledge of what has come before.”). Indeed, Petitioner relies on this principle in asserting that “a POSITA would have understood” from Perego’s description of control and address information that “Perego’s buffer device includes logic configured to output data buffer control signals.” Pet. 63.

As confirmed by Dr. Przybylski (EX2024, ¶¶ 82-83), a POSITA reading the ’087 Provisional and looking at Figure 1 would understand, based on knowledge of the art and contemporaneous JEDEC standards, *see* EX1005, [0006] (“The memory of certain embodiments comprises a DDR2 SDRAM memory array....”), [0022], that: 1) the disclosed DIMM has a 64-bit data bus; 2) each rank would be burst-oriented and input or output 64-bit bursts of data in response to read or write commands; 3) the RBDL would transfer these burst between the memory devices and the memory bus, EX1005, [0007]; 4) the “data path multiplexer/demultiplexer,” which is part of the RBDL circuitry and among other things “simplifies various ... aspects of operation of the memory module,” *id.*, [0008], would receive read or write commands (through command decode circuitry that a POSITA would understand to

receive commands from an external memory controller) and output data buffer control signals and transfer bursts of 64-bit wide data signals between the memory bus and the memory devices in response to those signals. EX2024, ¶¶ 82-83, 89-91. Thus, the '087 Provisional provides adequate written description support for the disputed claim limitations when considered “in the context of the particular invention and the state of the knowledge [in the art].” *Capon v. Eshhar*, 418 F.3d 1349, 1357-58 (Fed. Cir. 2005).

2. The Speculative Alternatives to Data Buffer Control Signals Proposed by Petitioner Are Not Viable

Petitioner contends that a POSITA would have recognized that data transfer through the '087 Provisional's buffer need not use data buffer control signals. Pet. 7-8. Petitioner proposes two alternative approaches that purportedly call into question the conclusions above. A POSITA would immediately understand that neither approach would work.

First, Petitioner proposes that “the data could be sent to both of the ranks, and a chip-select signal (e.g., rcs0#, rcs1#) could be used to target one of those ranks.” Pet. 8. But that would not apply to read commands, “during which the RBDL must select the data coming from the one addressed Rank and transfer it to the memory bus,” and for write commands, “the RBDL must understand when to forward data from the memory bus to the rank data buses.” EX2024, ¶ 84.

Second, Petitioner suggests that “data transfer through the buffer ... could be controlled by other means, such as the ‘preamble’ on the DQS strobe lines.” Pet. 8. As explained by Dr. Przybylski, “[t]he DQS preamble *cannot* be used to control the data transfer through the RBDL” because there may be preambles for burst data transfers for other ranks that the RBDL and in any event “the RBDL cannot identify the beginning of [a] preamble.” EX2024, ¶ 86. As Petitioner’s expert Dr. Wolfe acknowledged, the DQS signal is in a high-impedance state with an indeterminate voltage level between adjacent data burst transactions on the DQS signal traces. EX2033, 171:12-172:20; EX2024, ¶ 87. Because the DQS signal lacks a reliably discernable transition in voltage at the start of a preamble, a POSITA would recognize that the RBDL cannot control the data burst through the buffer in response to such preambles but instead would use data buffer control signals. EX2024, ¶ 88.

3. The ’087 Provisional Provides Support for the Remaining Limitations of the Challenged Claims

Petitioner bears the burden of proving unpatentability “and that burden never shifts to the patentee.” *Dynamic Drinkware v. Nat’l Graphics*, 800 F.3d 1375, 1378-79 (Fed. Cir. 2015); 35 U.S.C. § 316(e). Petitioner has asserted that the ’417 Patent is not entitled to a priority date of before July 1, 2005 because it purportedly does not provide support for “data buffer control signals” [1.c.4] that enable the transfer of data bursts through the buffer in response to read or write memory commands.

[1.e]. Pet. 5-9. Petitioner has put priority at issue and taken on the burden for why it believes that the '417 Patent is not entitled to a priority date before July 1, 2005. *See Polaris Wireless, Inc. v. TruePosition, Inc.*, IPR2013-00323, Paper 9 at 29 (PTAB Nov. 15, 2013). Netlist need only respond “commensurate in scope” to that “specific points and contentions” to rebut Petitioner’s position to prevail. *Lupin Ltd. v. Pozen, Inc.*, IPR2015-01775, Paper 15, at 10-11 (PTAB Mar. 1, 2016); *Focal Therapeutics, Inc. v. SenoRx, Inc.* IPR2014-00116, Paper 8 at 9-10 (PTAB Apr. 22, 2014); *Fitbit, Inc. v. BodyMedia, Inc.*, IPR2016-00707, Paper 9 at 10-11 (PTAB Sep. 8, 2016). There is no further burden on Netlist to show that ***all*** elements of ***all*** claims are present as Petitioner has not contested those other limitations, despite the clear opportunity to do so. This comports with the limited space in and rigid briefing order in IPR (in contrast to district court) and prevents unnecessary sandbagging in reply. *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1357 (2018) (Petition controls the “scope of the proceeding.”).

Nevertheless, Netlist provides the following chart of exemplary citations of where each of the challenged claims has support pre-dating Ellsberry viewed through the lens of a POSITA (*see* EX2024, ¶ 92):

Claim/Element	Exemplary Citations of Support
1.a.1	EX1005, [0001]-[0004], [0007]-[0008], [0010]-[0011], [0014]-[0015], [0016]
1.a.2	EX1005, Fig. 1, [0001], [0004]-[0005], [0007], [0009]-[0013]-[0018], [0021]; EX1006, [0019];

	EX1007 at [0015], 10, 14-16; EX1008 at [0015], 17, 21-23; EX1009, [0006]; EX1011, 4:65-66; 5:31-34, 8:58-62, 7:13-22, 33-36, 10:19-23, 10:34-37; 15:27-33, 17:17-21
1.a.3	EX1005, Fig. 1, [0010], [0018]; EX1007 at 9-11; EX1008 at 16-18
1.a.4	[1.a.1]
1.b	EX1005, Fig. 1, [0001], [0003]; EX1006, [0001], [0023], [0025]-[0026]; EX 1007, [0006], 9, 20, 22-23, 25-38; EX1008, [0001], [0007], [0019], APPX 1, [0006], 16, 27-44; EX1011, 1:22-25, 3:56-60, 7:50-54, 11:22-30, Fig. 5A-5B
1.c.1	[1.a.2], [1.a.3], [1.b] EX1005, Fig. 1, [0004]-[0011], [0014], [0016]-[0017]
1.c.2	[1.a.3] EX1005, [0005], [0008], [0009], [0017]; EX1006, Table 1, [0004]-[0005], [0009]-[0020], [0023]-[0026]; EX1007 at 10; EX1008 at 17; EX1011, 5:5-6, 6:51-55, 15:60-63, 17:31-45, 18:3-11
1.c.3	[1.c.1]-[1.c.2] EX1005, [0002], [0005], [0012], [0014]-[0016]; EX1006, Table 1, [0004]-[0005], [0009]-[0020], [0023]-[0026]; EX1007 at 10; EX1008 at 17; EX1009, [0008], [0010]-[0011]; EX1011, 5:5-6, 5:54-6:32, 6:51-55, 15:60-63, 17:31-45, 17:59-18:11
1.c.4	[1.a.2], [1.a.3], [1.c.1] See Przybylski Declaration. EX1005, Fig. 1, [0005], [0008], [0009], [0017]; EX1007 at 10; EX1008 at 17
1.d.1	[1.a.2], [1.b] EX1005, [0004]-[0010], [0015]
1.d.2	[1.c.2], [1.c.3], [1.d.1]

	EX1005, Fig. 1, [0005], [0008], [0009], [0017]
1.d.3	[1.a.2], [1.c.3], [1.d.1]-[1.d.2] EX1005, Fig. 1, [0005], [0008], [0009], [0017]; EX1007, [0015], 9-12 14-17; EX1008, [0015], 16-24; EX1008 at 16, 21, 24
1.e	[1.a.2]; [1.a.3], [1.c.1], [1.d.1], [1.d.3], [1.c.4] See Przybylski Declaration. EX1005, Fig. 1, [0005], [0008], [0009], [0017]; EX1007 at 10; EX1008 at 17
1.f	[1.e] EX1005, Fig. 1, [0005], [0008], [0009], [0017]; EX1007 at 10; EX1008 at 17
2	EX1005, Fig. 1, [0005], [0008]-[0009]
3	[1.c.4], [1.d.3], [1.e] EX1005, Fig. 1, [0017]; EX1007, [0015], 9-12 14-17; EX1008, [0015], 16-19., 21-24
4	[1.a.2], [1.d.1] EX1005, [0005], [0010], [0012], [0014]-[0016], [0019]; EX1006, [0002]; EX1007, 9-11; EX1008, [0004]-[0006], [0011]-[0014], Appx 1, 16-18; EX1011, 1:38-48, 1:57-65, 4:32-37, 4:54-59, 7:50- 54, 8:1-14, 8:52-55, 12:48-13:7, Table 1, 14:4-35, 15:21-25, 15:33-43, 15:55-59, Fig. 5A-5B, Fig. 9, Fig. 10A
5	[1.c.2], [1.d.1] EX1005, [0002], [0005], [0012], [0014]-[0016]; EX1006, [0003]-[0020], [0023]-[0026]; EX1007 at 10; EX1008 at 17; EX1009, [0008], [0010]-[0011]; EX1011, 5:5-6, 5:54-6:32, 6:51-55, 17:31-45, 17:59- 18:3-11
6	[1.e.], [1.f]

	EX1005, [0005], [0008], [0009], [0017]
7	[1.c.1], [1.c.4], [1.c.4], [1.e], [1.f] EX1005, Fig. 1, [0005], [0008], [0009], [0017]; EX1007, 10, 16; EX1008, 17, 23
8	[1.a.1], [1.a.2], [1.d.1], [1.d.3] EX1005, Fig. 1; EX1007, [0004], 9-10, 14-15; EX1008, [0006], Appx 1 [0004], 16-17, 21-22; EX1011, 7:29-33, 7:47-50, 10:30-34, 12:38-64, Table 1
9	[1.e.]-[1.f] EX1005, Fig. 1, [0005], [0008], [0009], [0017]; EX1006, [0009], Fig. 1; EX1007, 9-11, 17, 39; EX1008, 16-17, 24; EX1011, 7:54-56
10	[1.d.1], [1.d.3] EX1005, [0006], [0019], [0022]; EX1007, [0001], 9- 10, 15-16; EX1008 at [0006], Appx. 1, [0001], 16-17, 22-23; EX1009, [0001] [00013]; EX1011, 3:56-60, 7:47-67, 10:30-37, Figs. 5A-5B
11	[1.c.4], [1.d.3], [1.e] EX1005, [0005], [0008], [0009], [0017]
12	[1.c.4], [1.d.3], [1.e], [11] EX1005, Fig. 1, [0005], [0008]-[0009]
13	[2]
14	[8]
15	[3]

C. Petitioner Has Not Demonstrated a Motivation to Combine Perego and JESD79-2 with Ellsberry

Even if the Board accepts Petitioner's priority-date arguments, Ellsberry cannot cure the deficiencies already identified with respect to Ground 1 because Petitioner fails to establish that a POSITA would have been motivated to combine Ellsberry's teachings with those of Ground 1. EX2024, ¶¶ 196-204.

Petitioner suggests that the relevance of JEDEC standards to both references would motivate the combination (Pet. 114), but while Ellsberry's discloses memory devices and modules aligned with JEDEC standards (*see* EX1073, [0008], [0009], [0026], [0046]), Perego discloses only the use of JEDEC-standardized memory devices through the use of protocol translation in the buffer of a module having a Rambus-style interface (*e.g.*, EX1071, 10:63-67). EX2024, ¶¶ 200-01. As discussed above, a POSITA would not be motivated to modify Perego's primary channel to conform with JEDEC standards. *See* Section VI.A, *supra*. Nor does Petitioner explain how or why a POSITA would combine the teachings of Ellsberry and Perego in view of the significant differences between their architectures and the tradeoffs involved in removing Perego's point-to-point interface, configurable primary channel width, and support for disparate memory devices. *See* Pet. 111-15; EX2024, ¶ 203; *Univ. of Md. Biotechnology Inst.*, 711 F. App'x at 1011; *Ratti*, 270 F.2d at 813.

Petitioner also asserts that one would look to Ellsberry's teaching of rank multiplication, which could be applied to Perego's memory module. Pet. 114. This makes little sense in view of the same Petitioner's assertion that Perego's module "implements rank multiplication." Pet. 91. In any event, Perego does not teach rank multiplication. Unlike Ellsberry (*see* EX1073, [0026]), Perego does not suggest "that the memory controller is presented with a view of the memory system in which it appears to the memory controller that two or more memory devices are actually one larger device." EX2024, ¶ 182. The Perego disclosures cited by Petitioner (Pet. 91) relate to target subsets of channels, apply only to non-JEDEC-standardized modules, and use Perego's configurable-width buffer to identify and route transactions using less than the full width of a channel. EX2024, ¶¶ 182-83; EX1071, 7:30-64, 11:56-12:3, 14:63-65, 15:31-42.

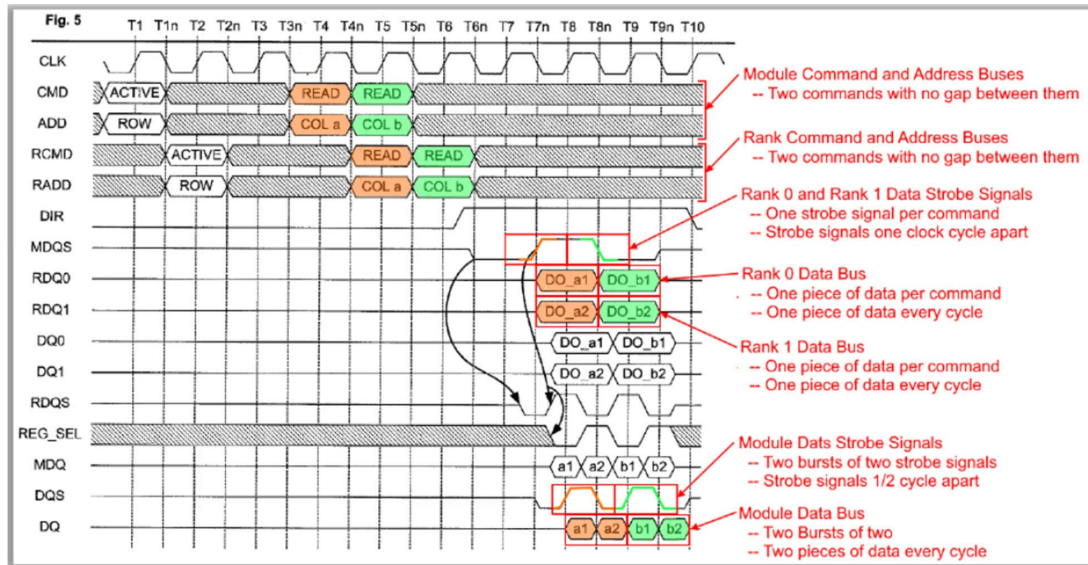
Petitioner also suggests that a POSITA would combine Perego and Ellsberry because both buffer data signals on the module. Pet. 114-15. Petitioner notes that Perego discloses a centralized buffer while Ellsberry discloses a distributed buffer architecture but fails to address the significant differences in these approaches. *See, e.g.,* EX2010, 2 (IDT comparison of DDR3 LRDIMM's centralized buffer and DDR4 LRDIMM's distributed buffer). Petitioner also ignores the vast difference between Ellsberry simply buffering DQ signals on the module (EX1073, [0012], [0047], Figs. 5, 6) and Perego's use of a configurable width buffered module to alter

the “memory system architecture/interconnect topology” (EX1071, Abstract). EX2024, ¶ 202. More fundamentally, Petitioner fails to explain why, when both references describe their memory modules and data buffers in such detail, a POSITA would be motivated to look elsewhere for implementation details. *See Monarch Knitting Mach. Corp. v. Sulzer Morat GmbH*, 139 F.3d 877, 880 (Fed. Cir. 1998) (rejecting attempt to define a problem in terms of its solution, which “reveals improper hindsight in the selection of the prior art relevant to obviousness”).

VIII. PETITIONER HAS NOT SHOWN OBVIOUSNESS UNDER GROUND 3

Halbert does not cure the deficiencies of Perego in view of JESD79-2. EX2024, ¶¶ 208-17. In fact, Halbert lacks many of the same claimed features as Perego and does not disclose, for example, “a plurality of N-bit wide ranks” [1.d.1] or input chip-select signals with different values [1.c.2] corresponding to registered chip-select signals with different values [1.c.3]. While Figure 4 of Halbert depicts two items 140 and 142 characterized as separate “ranks” in the specification (*e.g.*, EX1078, 4:52-55), that description is not consistent with Petitioner’s proposed construction of “rank” in this proceeding. *See* Pet. 26. Instead of receiving and responding to separate registered chip-select signals as required by the claims, “ranks” 140 and 142 “are together part of a singular memory device array that receives a single registered address and command bus (RADD/RCMD).” EX2024,

¶ 212; EX1078, Fig. 4. The two collections of memory devices always receive identical chip-select signals because they behave identically, as shown in Figure 5 (annotated) below. EX2024, ¶ 212.



EX1078, Figure 5, Annotated. That is consistent with Halbert’s disclosure, which explains that “[g]enerally, *multiple ranks will receive the same address and commands*, and will perform memory operations with the interface circuit concurrently.” *Id.*, 4:57-59; EX2024, ¶¶ 212-14. Dr. Wolfe agreed that “ranks” 140 and 142 collectively constitute a single rank under Petitioner’s proposed construction. EX2033, 162:4-163:23. He later attempted to hedge that statement after being reminded of Halbert’s use of the word “generally,” after which he testified that they would constitute two ranks “if they receive different commands.” *Id.*, 179:20-180:16. The Petition, however, identifies no disclosure in Halbert where “ranks” 401 and 402 receive different commands. *See* Pet. 120-26; EX2024, ¶ 214

(noting additionally that Fig. 2 depicts prior art incompatible with Halbert).

Regarding the limitations related to data transfer delay and CAS latency [1.e.3], [1.f], and [9], Petitioner fails even to allege disclosure of the full claimed requirements. As discussed above, [1.f] explicitly requires data transfers to be registered through the claimed circuitry between the memory devices and the external controller. Thus, the claimed time delay must include delay in the data path; delay on the address/control path alone cannot will not suffice. EX2024, ¶ 217. Petitioner alleges that Halbert Figs. 3 and 4 render obvious a memory module with an overall CAS latency that is greater than an actual operational CAS latency of each of each of the memory devices by at least one clock cycle, Pet. 124-26, but fails to address whether or not the “data transfers through the circuitry are registered for an amount of time delay” as required by Claim 1. Petitioner cites several paragraphs of Dr. Wolfe’s declaration without explanation, Pet. 124, but he relies on Halbert “registering the *address and command signals*” and the resultant delay. *E.g.*, EX1003, ¶ 366 (citing EX1078, 2:46-55); *see also* EX2024, ¶217; Pet. 125 (showing that Petitioner relies on the delay in the control path between a command being presented on ADD/CMD and emerging onto RADD/RCMD). As with the JESD21-C note cited by Petitioner, that disclosure of registered address/command signals is irrelevant to this claim element. *See* Section VI.C, *supra*.

IX. PETITIONER HAS NOT ESTABLISHED SIMULTANEOUS INVENTION

Finally, Petitioner asserts that Ellsberry, Perego, and an additional reference Amidi (EX1079) not asserted in this IPR, as well as other patents within the same family as the '417 Patent, demonstrate “simultaneous invention” as a secondary consideration of obviousness. Pet. 126-27. Petitioner’s argument rests on the false premise that these other references and patents “recognized and solved the same problem” as the '417 Patent through “rank multiplication.” *Id.* The '417 Patent does not claim “rank multiplication” (*see* EX1001, 42:7-44:33; EX2024, ¶ 78), however, which defeats Petitioner’s claim. Furthermore, Perego does not even disclose rank multiplication. *See* Section VII.C, *supra*; EX2024, ¶¶ 160-61. Petitioner has not established any contemporaneous invention of the subject matter actually claimed in the '417 Patent. EX2024, ¶¶ 218-19. Rank multiplication alone is insufficient to show simultaneous invention, which must be of the actual invention and cover the complete claim. *Immunex Corp. v. Sandoz, Inc.*, 964 F.3d 1049 (Fed. Cir. 2020) (no simultaneous invention when the evidence relates to unclaimed proteins); *Endo Pharms. Inc. v. Actavis LLC*, 922 F.3d 1365 (Fed. Cir. 2019) (invention not obvious because the alleged simultaneous invention related to unclaimed oxycodone). The absence of any even allegedly anticipatory references shows that there was no simultaneous invention.

X. CONCLUSION

Based on the foregoing, the Board should decline to find the challenged claims of the '417 Patent unpatentable.

Dated: December 8, 2023

Respectfully submitted,

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CERTIFICATE OF WORD COUNT

I hereby certify, pursuant to 37 C.F.R. section 42.24, that the foregoing Patent Owner Response contains 11,574 words, excluding the words in the table of contents, table of authorities, mandatory notices under section 42.8, this certificate of word count, certificate of service or exhibit list. The word count is based on the word count of the Microsoft Word program used to prepare the Patent Owner Preliminary Response.

/Philip Warrick/
Philip Warrick, (Reg. No. 54,707)
)

CERTIFICATE OF SERVICE

I hereby certify, pursuant to 37 C.F.R. section 42.6, that on December 8, 2023, a complete copy of the **PATENT OWNER'S RESPONSE and EXHIBITS 2024-2035** were served upon the following, by ELECTRONIC MAIL:

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